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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 1046.1188/JDH

First Named Inventor or Application Identifier:

Shigeki HAMURA, et al.

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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2. [X] Specification, Claims & Abstract ..... [Total Pages: 37]
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NEW APPLICATION FEE TRANSMITTAL		Attorney Docket No.	1046.1188/JDH
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Signature		Date	August 24, 1998

PRINTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a printer printing an image corresponding to print data outputted from computer.

2. Description of the Related Art

Conventionally, there is one of printers, which is provided with an image buffer stored with print data outputted from computer, and prints data by transferring the print data stored in this image buffer to a print mechanism in sequential.

FIG. 12 shows a control circuit in such a conventional printer. As shown in FIG. 12, the control circuit in the conventional printer is provided with a communication interface 20, a MPU (micro processing unit) 21, an image buffer 22, a VIF (video interface) 23, an image processing circuit 24, and a print mechanism 25 connected through a control bus B1 one another. Further, the communication interface 20, the MPU 21, the image buffer 22 and the VIF 23 are connected through a data bus B2 one another.

The MPU 21 is a processing unit controlling an action of each circuit block through the control bus B1.

The communication interface 20 receives the print data transmitted from host computer (not shown), and transmits the print data into the data bus B2. This

print data is transmitted from computer (or server), and includes character codes, image dot data, printer setting data, commands and the like.

The image buffer 22 is a memory temporarily storing the print data individually transmitted to the data bus B2 from the communication interface 20 in accordance with the control of the MPU 21.

The VIF 23 reads one piece of print data stored in the image buffer 22, and outputs the read print data to the image processing circuit 24 as an image signal which is data from the printer, namely, a video signal, in accordance with the control of the MPU 21. The VIF 23 receives a synchronous signal from the print mechanism 25 when outputting the image signal to the image processing circuit 24, and outputs the image signal in synchronous with this synchronous signal. Further, when the VIF 23 reads a new piece of print data, it is necessary for the MPU 21 to set an address and so on concerning the print data to be read in the image buffer 22.

The image processing circuit 24 applies various image processes set by the MPU 21 to the image signal outputted from the VIF 23, and then outputs the image signal to the print mechanism 25.

The print mechanism 25, based on the image signal received from the image processing circuit 24, prints an image corresponding to this image signal. The print

mechanism 25 gives the synchronous signal to the VIF 23.

As above described, the control circuit in the conventional printer is provided with only one set of the VIF 23 and the image processing circuit 24. Therefore, there are three problems as follows.

The first problems in the conventional printer is explained. Since the control circuit in the conventional printer is provided with only one VIF 23, only an image corresponding to one piece of print data can be printed concerning one page. For example, in order to print a text (data) in a prescribed form, when print data corresponding to the text and print data corresponding to the prescribed form are transmitted from host computer, the MPU 21 previously integrates two pieces of print data into one piece of print data with a software process, and then stores it in the image buffer 22. In this way, the VIF 23 is capable of printing the text (data) on the prescribed form only by reading one piece of integrated print data from the image buffer 22. However, there is a problem in that the printer operates slowly because the integration process of print data gives a big load to the MPU 21.

The second problem in the conventional printer is explained. Since the control circuit in the conventional printer is provided with only one VIF 23, this VIF 23 must read all of print data. For example, in a case of a printer having a buffer memory of which capacity is

smaller than one page and performing band printing, the VIF 23 must read all bands of print data every in sequence transmitted from the host computer. Then, the VIF 23 must be reset by the MPU 21 in order to read a new piece of band print data. During the resetting, the VIF 23 must stop. Accordingly, there is a problem in that the image printed by the print mechanism 25 brakes off when a time necessary to reset the VIF 23 exceeds an allowed time (a time necessary to output all picture signals in a buffer in the VIF 23).

The third problems in the conventional printer is explained. Since the control circuit in the conventional printer is provided only one image processing circuit 24, one kind of image process concerning one page is able to be executed. However, in a case of that print data includes text data and image data, it is desirable that an image processing suitable to the text data is applied to the text data while it is desirable that an image processing suitable to image data is applied to the image data. For example, it is desirable to apply the smoothing process to the text data while it is desirable to apply the intermediate tone process to the image data. Further, concerning the resolution of the image, in order to execute high-speed printing, it is desirable to apply the low-resolution process to the text data while it is desirable to apply the high resolution process to the image data. Moreover,

concerning data compression/decompression, it is desirable that, as to the text data, the run-length compression is executed in the host computer and then the run-length decompression is executed in the image processing circuit 24, while it is desirable that, as to the image data, the LZ compression is executed in the host computer and then the LZ decompression is executed in the image processing circuit 24. In spite of such a request for the control circuit in the conventional printer, there is a problem in that only one image process suitable to text data or image data is applied to the print data since there is only one image processing circuit 24.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to solve the problems in the conventional printer, and to provide a printer capable of individually processing a plurality of print data corresponding to parts of an image to be printed on one page and capable of printing the image on one page based on these print data.

To solve the above-mentioned problems, the present invention introduces the following aspects.

That is, the first aspect according to the present invention is a printer outputting a plurality of print data corresponding to am image to be printed on a same

page, each of the print data having an attribute. The printer is provided with an image buffer storing each of the print data in accordance with the attribute, a plurality of video interfaces, each of said video interfaces reading each of said print data stored in the image buffer, a print data integration circuit integrating the plurality of print data read by the video interfaces into a piece of print data for the same page, and an output mechanism outputting the image of the same page based on the print data integrated by the print data integration circuit.

With this arrangement, the image buffer stores a plurality of print data to be printed on the same page in accordance with the attribute. Each video interface reads one of print data stored in the image buffer independently of another video interface. Accordingly, it is possible to apply a peculiar process to each of print data read by each video interface. Then, these print data are integrated by the print data integration circuit. The output mechanism outputs the image on the same page based on the print data integrated by the print data integration circuit.

A print of the second aspect is specified by that the plurality of print data stored in the image buffer contain form print data corresponding to a form and text print data corresponding to a text to be printed over the form.

A printer of the third aspect, in addition to the first aspect, comprises a separation unit for separating print data corresponding to an image with an text into print data corresponding to the image and print data corresponding to the text, and a storage unit for storing each of the print data separated by said separation means in the image buffer in accordance with the attribute.

A printer of the fourth aspect, in addition to the third aspect, further comprises a plurality of image processing circuits, each of said image processing circuits applying each image process to each of the print data read by each of said video interfaces.

A printer of the fifth aspect is specified by that the plurality of print data stored in the image buffer are obtained by dividing print data corresponding to the image to be printed on the same page into a plurality of bands, and wherein said print data integration circuit repeatedly selects each of said print data read by each of said video interfaces and outputs selected print data to the output mechanism.

The present invention may be a controller controlling a plurality of print data, each of the print data having an attribute. The controller is provided with, a plurality of video interfaces, each of said video interfaces reading each of said print data stored in the image buffer storing each of the print data in

accordance with the attribute, and a print data integration circuit integrating the plurality of print data read by the video interfaces into a piece of print data for the same page.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a configuration of a control circuit in a printer according to an embodiment of the present invention;

FIG. 2 is a flowchart showing a control process executed by the MPU 2 in Operational Example 1;

FIG. 3 is an explanatory view showing an operation of a printer in Operational Example 1;

FIG. 4 is a flowchart showing a control process executed by the MPU 2 in Operational Example 2;

FIG. 5 is an explanatory view showing an operation of a printer in Operational Example 2;

FIG. 6 is a flowchart showing a control process executed by the MPU 2 in operational Example 3;

FIG. 7 is an explanatory view showing an operation of a printer in Operational Example 3;

FIG. 8 is a flowchart showing a control process executed by the MPU 2 in Operational Example 4;

FIG. 9 is an explanatory view showing an operation of a printer in Operational Example 4;

FIG. 10 is a flowchart showing a control process

executed by the MPU 2 in Operational Example 5;

FIG. 11 is an explanatory view showing an operation of a printer in Operational Example 5; and

FIG. 12 is a block diagram showing a configuration of a control circuit in a conventional printer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, concrete explanations are given of embodiments of the present invention with reference to drawings.

First, an explanation will be given of a control circuit in a printer according to an embodiment of the present invention.

FIG. 1 is a block diagram showing the control circuit in the printer according to the embodiment of the present invention. As shown in FIG. 1, the control circuit of the printer according this embodiment is provided with a communication interface 1, a MPU (micro processing unit) 2, an image buffer 3, first through n-th VIFs (video interface) 4-1 through 4-n, first through n-th image processing circuits 5-1 through 5-n, a selection integration circuit 6, and a print mechanism 7 connected through a control bus B1 one another. Further, the communication interface 1, the MPU 2, the image buffer 3, and each of the VIFs 4-1 through 4-n are connected through a data bus B2 one another. The first VIF 4-1 is connected with the image processing circuit

5-1 through a data line D, and the second VIF 4-2 is connected to the image processing circuit 5-2 through a data line D. Similarly, the n-th VIF 4-n is connected to the n-th image processing circuit 5-n through a data line D. Each of the image processing circuits 5-1 through 5-n is also connected to the selection integration circuit 6 through a data line D. The selection integration circuit 6 is also connected to the print mechanism 7 through a data line D. The print mechanism 7 is connected to each of the VIFs 4-1 through 4-n through a signal line S.

The communication interface 1 receives print data transmitted from host computer (not shown), and transmits the print data into the data bus B2. This print data is transmitted from computer (or server), and includes character codes, image dot data, printer setting data, commands and the like.

The MPU 2 is a central processing unit controlling an action of each circuit through the control bus B1. Concretely, the MPU 2 transmits an address and an command to each circuit in the printer through the control bus B1, thereby storing the print data transmitted to the data bus B2 by the communication interface 1 into one of the storage areas "image 1" through "image n" of a predetermined address in the image buffer 3, setting each of the VIFs 4-1 through 4-n, setting description of image processing to be

executed by each of the image processing circuits 5-1 through 5-n, setting whether the selection integration circuit 6 should execute the selection action or the integration action, and instructing a printing start to the print mechanism 7. Incidentally, the selection integration circuit 6 executes three functions such as image data selection, image data integration and combination of them. The MPU 2 instructs the selection integration circuit 6 to execute one function among these three functions.

Further, when print data transmitted to the data bus B2 by the communication interface 1 includes text data and image data, the host computer generates this print data so as to be distinguished between text data and image data, namely, so as to be distinguished based on the attribute. Thus, the MPU 2 divides this print data into text data and image data (corresponding to a separation unit), and stores the divided pieces of data in the image buffer 3 independently (corresponding to a storage unit).

The image buffer 3 is a memory temporarily storing each print data transmitted into the data bus B2 by the communication interface 1 or the MPU 2 in a positions corresponding to an address appointed by the MPU 2 through the control bus B1.

Each of the VIFs 4-1 through 4-n is instructed by the MPU 21 through the control bus B1, and reads print

data from the position of the address appointed by this instruction in the image buffer 3. Then, each of the VIFs 4-1 through 4-n outputs the read print data as an image signal to each of the image processing circuits 5-1 through 5-n connected to itself. Incidentally, each of the VIFs 4-1 through 4-n, when outputting the image signal to each of the image processing circuits 5-1 through 5-n, receives a synchronous signal from the print mechanism 7 and outputs image signals for several lines in synchronous with the synchronous signal.

Each of the image processing circuits 5-1 through 5-n applies various image processes instructed by the MPU 2 to the image signal outputted from one of the VIFs 4-1 through 4-n connected to itself, and then outputs the image signal to the print mechanism 25. As the image process capable of being executed by each of the image processing circuits 5-1 through 5-n, there are the smoothing process for text data (process making notches at peripheries of bit map font constituting character into smooth slanted lines or curves), the intermediate tone process for image data (process smoothing variation of light and shade in the image), the low-resolution process for text data (process reducing a number of dots constituting character), the high-resolution process for image data (process making pixels constituting image fine), the run-length decompression process for the run-length compressed text data, and the LZ decompression

process for the LZ compressed image data.

The selection integration circuit 6 as a print data integration unit, when a selection action is instructed by the MPU 2 through the control bus B1, selects an image signal from one image processing circuit 5 appointed by the MPU 2 and transmits it to the print mechanism 7, and when transmission of the image signal from this image processing circuit 5 terminates, selects an image signal from another image processing circuit 5 appointed by the MPU 2 and transmits it to the print mechanism 7. In this way, when the selection action is instructed, the selection integration circuit 6 selects image signals from two image processing circuits 5 appointed by the MPU 2, integrates them as an image signal (print data) for one page, and transmits it to the print mechanism 7. Further, the selection integration circuit 6, when a integration action is instructed by the MPU 2 through the control bus B1, integrates image signals from a plurality of image processing circuits 5 appointed by the MPU 2 into one image signal so as to integrate them into print data for one page, and transmits this image signal to the print mechanism 7.

The print mechanism 7, based on the image signal received from the selection integration circuit 6, prints an image corresponding to this image signal on a sheet of paper. The print mechanism 7 gives synchronous

signals to all VIFs 4-1 through 4-n outputting image signals selected or integrated by the selection integration circuit 6.

Next, explanations will be given of controls (namely, action of the printer) actually executed by the MPU 2 every kind of print data transmitted from host computer not shown as operational examples 1 through 5.

<Operational Example 1>

The operational example 1 shows a control process (action of the printer) executed when print data for printing an image of a text (hereinafter, called "text print data") and print data for printing an image of a form (hereinafter, called "form print data") are transmitted from the host computer not shown in order to execute the form printing (overlay printing).

FIG. 2 is a flowchart showing this control process, and FIG. 3 is an explanatory view showing an action in the printer when the MPU 2 executes the control process according to this flowchart.

The flowchart in FIG. 2 starts with that the communication interface 1 receives print data transmitted from host computer not shown. After starting, the MPU 2 transmits the text print data (code or image data) to the image buffer 3 from the communication interface 1 (S01), and transmits the image print data to the image buffer 3 from the communication interface 1 (S02). At this time the MPU 2, as shown in

FIG. 4, stores the text print data in a position 3a indicated by the first address in the image buffer 3 (hereinafter, called "the first address position"), and stores the form print data in a position 3b indicated by the second address in the image buffer 3 (hereinafter, called "the second address position"). Incidentally, the order of S01 and S02 may be reversed.

In the next S03, the MPU 2 instructs the first VIF 4-1 to read print data from the first address position 3a in the image buffer 3 and instructs the second VIF 4-2 to read print data from the second address position 3b in the image buffer 3.

In the next S04, the MPU 2 instructs the selection integration circuit 6 to executes the integration action.

In the next S05, the MPU 2 instructs the first and second VIFs 4-1 and 4-2, the first and second image processing circuits 5-1 and 5-2, the selection integration circuit 6, and the print mechanism 7 to start printing. The first VIF 4-1, when receiving the instruction, reads the text print data from the first address position in the image buffer 3 and transmits image signals for several lines to the selection integration circuit 6 through the first image process circuit 5-1. At the same time, the second VIF 4-2 reads the form print data from the second address 3b in the image buffer 3 and transmits image signals for several

lines to the selection integration circuit 6 through the second image process circuit 5-2. The selection integration circuit 6 integrates the image signals received through the first and second image processing circuits 5-1 through 5-2, and transmits the integrated image signal to the print mechanism 7. The print mechanism 7 prints the image corresponding to the image signal received from the selection integration circuit 6 on a sheet of paper. After this printing, the print mechanism 7 transmits the synchronous signal to both the first and second VIFs 4-1 and 4-2. The first and second VIFs 4-1 4-2, which receive this synchronous signal, transmit image signals to the selection integration circuit 6 so long as there is an image signal not yet transmitted.

In the next S06, the MPU 2 waits until the first and the second VIFs 4-1 and 4-2 transmit all image signals corresponding to print data (namely, until the print mechanism 7 finishes the printing). When transmission of all image signals corresponding to print data is finished (namely, when printing by the print mechanism 7 is finished), the MPU 2 terminates this control process.

In this way, according to the operational example 1, not software process in the MPU 2 but the hardware action in the selection integration circuit 6 integrates text data and form data for the form printing.

Accordingly, there is no need of a time required to integrate text print data and form print data by the MPU 2, therefore, the printing by the print mechanism 7 is executed in real time as to transmission of print data from host computer.

<Operational Example 2>

The operational example 2 shows the control process (action of a printer) executed in order to execute print when print data including text data and image data is transmitted.

FIG. 4 is a flowchart showing this control process, and FIG. 5 is an explanatory view showing an action in the printer when the MPU 2 executes the control process according to this flowchart.

The flowchart in FIG. 4 starts with that the communication interface 1 receives print data transmitted from the host computer not shown. In the first S10 after starting, the MPU 2 reads print data from the communication interface 1.

In the next S11, the MPU 2 divides the read print data into print data corresponding to a text part (hereinafter, called "text print data) and print data corresponding to an image part (hereinafter, called "image print data") based on the attribute shown in the print data transmitted from the computer (equivalent to a separation unit).

In the next S12, the MPU 2 transmits the text print

data and the image print data to the image buffer 3. At that time, the MPU 2, as shown in FIG. 5, stores the text print data in a position 3a indicated by the first address in the image buffer 3 (hereinafter, called "the first address position") and stores the image print data in a position 3b indicated by the second address in the image buffer 3 (hereinafter, called "the second address position") (equivalent to a storage unit).

In the next S13, the MPU 2 instructs the VIF 4-1 to read print data from the first address position 3a in the image buffer 3, and instructs the second VIF 4-2 to read print data from the second address position 3b in the image buffer 3.

In the next S14, the MPU 2 instructs the first image processing circuit 5-1 for the text part to executes the smoothing process.

In the next S15, the MPU 2 instructs the second image processing circuit 5-2 for the image part to execute the intermediate tone process.

In the next S16, the MPU 2 instructs the selection integration circuit 6 to execute the integration action.

In the next S17, the MPU 2 instructs the first and second VIFs 4-1 and 4-2, the first and second image processing circuits 5-1 and 5-2, the selection integration circuit 6, and the print mechanism 7 to start the printing. The first VIF 4-1, when receiving this instruction, reads the text print data from the

first address position 3a in the image buffer 3 and transmits image signals for several lines to the first image processing circuit 5-1. At the same time, the second VIF 4-2 reads the image print data from the second address position 3b in the image buffer 3 and transmits image signals for several lines to the second image processing circuit 5-2. The first image processing circuit 5-1, which receives the image signals, transmits them to the selection integration circuit 6 after applying the smoothing process to the image signals. On the other hand, the second image processing circuit 5-2, which receives the image signals, transmits them to the selection integration circuit 6 after applying the intermediate tone process to the image signals. The selection integration circuit 6 integrates image signals received from the first and second image processing circuits 5-1 and 5-2 and transmits the integrated image signal to the print mechanism 7. The print mechanism 7 prints the image corresponding to the image signal received from the selection integration circuit 6 on a sheet of paper. After this printing, the print mechanism 7 transmits the synchronous signal to the first and second VIFs 4-1 and 4-2 as above described. The first and second VIFs 4-1 and 4-2, which receive the synchronous signal, transmit image signals of the next line to the selection integration circuit 6 so long as there is an image signal not yet transmitted.

In the next S18, the MPU 2 waits until the first and second VIFs 4-1 and 4-2 transmit all image signals corresponding to print data (namely, the print mechanism 7 terminates the printing). When transmission of all image signals corresponding to print data is finished (when the print mechanism 7 finishes the printing), the MPU 2 terminates this control process.

In this way, according to the operational example 2, it is possible to divide print data received from host computer into a plurality of parts according to a kind of image, and to execute an image process which differs every divided part. Then, the print data to which respective image processes are applied are integrated into an image signal for one page and printed on a sheet of paper.

<Operational Example 3>

The operational example 3 shows a control process (action of the printer) executed in order to print data in the most suitable resolution when the print data including both text data and image data is transmitted.

FIG. 6 is a flowchart showing this control process, and FIG. 7 is an explanatory view showing an action in the printer when the MPU 2 executes the control process according to this flowchart.

The flowchart in FIG. 6 starts with that the communication interface 1 receives print data transmitted from the host computer not shown. In the

first S20 after starting, the MPU 2 reads print data from the communication interface 1.

In the next S21, the MPU 2 divides the read print data into print data corresponding to a text part (hereinafter, called "text print data) and print data corresponding to an image part (hereinafter, called "image print data") (equivalent to a separation unit).

In the next S22, the MPU 2 transmits the text print data and the image print data to the image buffer 3. At that time, the MPU 2, as shown in FIG. 7, stores the text print data in a position 3a indicated by the first address in the image buffer 3 (hereinafter, called "the first address position") and stores the image print data in a position 3b indicated by the second address in the image buffer 3 (hereinafter, called "the second address position") (equivalent to a storage unit).

In the next S23, the MPU 2 instructs the first VIF 4-1 to read print data from the first address position 3a in the image buffer 3, and instructs the second VIF 4-2 to read print data from the second address position 3b in the image buffer 3.

In the next S24, the MPU 2 instructs the first image processing circuit 5-1 for the text part to execute the low-resolution process.

In the next S25, the MPU 2 instructs the second image processing circuit 5-2 for the image part to execute the high-resolution process.

In the next S26, the MPU 2 instructs the selection integration circuit 6 to execute the integration action.

In the next S27, the MPU 2 instructs the first and second VIFs 4-1 and 4-2, the first and second image processing circuits 5-1 and 5-2, the selection integration circuit 6, and the print mechanism 7 to start the printing. The first VIF 4-1, when receiving this instruction, reads the text print data from the first address position 3a in the image buffer 3 and transmits image signals for several lines to the first image processing circuit 5-1. At the same time, the second VIF 4-2 reads the image print data from the second address position 3b in the image buffer 3 and transmits image signals for several lines to the second image processing circuit 5-2. The first image processing circuit 5-1, which receives the image signal, transmits the image signal to the selection integration circuit 6 after applying the low-resolution process to the image signal. On the other hand, the second image processing circuit 5-2, which receives the image signal, transmits the image signal to the selection integration circuit 6 after applying the high-resolution process to the image signal. The selection integration circuit 6 integrates image signals received from the first and second image processing circuits 5-1 and 5-2, and transmits the integrated image signal to the print mechanism 7. The print mechanism 7 prints the image corresponding to

the image signal received from the selection integration circuit 6 on a sheet of paper. After this printing, the print mechanism 7 transmits the synchronous signal to the first and second VIFs 4-1 and 4-2 as above described. The first and second VIFs 4-1 and 4-2, which receive the synchronous signal, transmit image signals of the next line to the selection integration circuit 6 so long as there is an image signal not yet transmitted.

In the next S28, the MPU 2 waits until the first and second VIFs 4-1 and 4-2 transmit all image signals corresponding to print data (namely, until the printing by the print mechanism 7 is finished). The MPU 2 terminates this control process when transmission of all picture signals corresponding to print data terminates (namely, when the printing by the print mechanism 7 is finished).

In this way, according to the operational example, it is possible to divide the print data received from the host computer into a plurality of parts according to kinds of images, and to execute an image process which differs every divided part. Then, the print data to which the respective image processes are applied are integrated into an image signal for one page, and printed on a piece of paper.

<Operational Example 4>

The operational example 4 shows a control process (action of the printer) executed in order to execute a

decompression process corresponding to each compression method when compressed print data including a text part to which the run-length compression process is applied and an image part to which the LZ compression process is applied is transmitted.

FIG. 8 is a flowchart showing this control process, and FIG. 9 is an operational explanatory view showing an action in the printer when the MPU 2 executes the control process according to this flowchart.

The flowchart in FIG. 8 starts with that communication interface 1 receives the compressed print data transmitted from the host computer not shown. In the first S30 after starting, the MPU 2 reads compressed print data from the communication interface 1.

In the next S31, the MPU 2 separates the read compressed print data into compressed print data corresponding to a text part (hereinafter, called "text compressed print data") and compressed print data corresponding to an image part (hereinafter, called "image compressed print data") (equivalent to a separation unit).

In the next S32, the MPU 2 transmits the compressed text print data and the compressed image print data to the image buffer 3. At that time, the MPU 2, as shown in FIG. 9, stores the compressed text print data in a position 3a indicated by the first address in the image buffer 3 (hereinafter, called "the first address

position") and stores the compressed image print in a position 3b indicated by the second address in the image buffer 3 (hereinafter, called "the second address position") (equivalent to a storage unit.

In the next S33, the MPU 2 instructs the first VIF4-1 to read compressed print data from the first address position 3a in the image buffer 3, and instructs the second VIF 4-2 to read compressed print data from the second address position 3b in the image buffer 3.

In the next S34, the MPU 2 instructs the first image processing circuit 5-1 for the text part to execute the run-length decompression process.

In the next S35, the MPU 2 instructs the second image processing circuit 5-2 for the image part to execute the LZ decompression.

In the next S36, the MPU 2 instructs the selection integration circuit 6 to execute the integration process.

In the next S37, the MPU 2 instructs the first and second VIFs 4-1 and 4-2, the first and second image processing circuits 5-1 and 5-2, the selection integration circuit 6, and the print mechanism 7 to start a printing. The first VIF 4-1, when receiving this instruction, reads the compressed text print data from the first address position 3a in the image buffer 3 and transmits the image signals for several lines to the image processing circuit 5-1. At the same time, the

second VIF 4-2 reads the compressed image print data from the second address position 3b in the image buffer 3, and transmits the image signals for several lines to the second image processing circuit 5-2. The first image processing circuit 5-1, which receives an image signal, transmits it to the selection integration circuit 6 after applying the run-length decompression process to this image signal. On the other hand, the second image processing circuit 5-2, which receives a image, transmits it to the selection integration circuit 6 after applying the LZ decompression process to this image signal. The selection integration circuit 6 integrates image signals received from the first and second image processing circuits 5-1 and 5-2, and transmits the integrated image signal to the print mechanism 7. The print mechanism 7 prints the image corresponding to the image signal received from the selection integration circuit 6 on a sheet of paper. After this printing, the print mechanism 7 transmits the synchronous signal to the first and second VIFs 4-1 and 4-2 as above described. The first and second VIFs 4-1 and 4-2, which receive the synchronous signal, transmit an image signal of the next line to the selection integration circuit 6 so long as there is an image signal not yet transmitted.

In the next S38, the MPU 2 waits until the first and second VIFs 4-1 and 4-2 transmit all image signals

corresponding to print data (namely, the printing by the print mechanism 7 is finished). Then, the MPU 2 terminates this control process when transmission of all image signals corresponding to print data is finished (namely, when the printing by the print mechanism 7 is finished).

In this way, according to the operational example 4, though print data including various images of which properties are different one another in one page is transmitted to a printer, the print data is divided into a plurality of parts according to the properties of the images and is compressed by suitable processes according to the properties of the images in the respective parts, whereby it becomes possible to make a size of print data smaller and to transmit the small print data to a printer. Accordingly, it is possible to shorten a time necessary for transmission of the print data. In the printer, the print data is divided every property, and independently stored in the image buffer 3. Then, a decompression process corresponding to the compression process applied to each part by each image processing circuit 5 is applied to each part, whereby an original image is restored. Thereafter, the restored images are integrated into an image for one page, and printed on a sheet of paper.

<Operational Example 5>

The operational example 5 shows a control process

(action of the printer) executed when print data (hereinafter, called "band print data") obtained by dividing print data for one page every band in order to execute the band printing is transmitted from host computer not shown.

FIG. 10 is a flowchart showing this control process, and FIG. 11 is an operational explanatory view showing an action in the printer when the MPU 2 executes the control process according to this flowchart.

The flowchart in FIG. 10 starts with that the communication interface 1 receives the first band print data transmitted from the host computer not shown. In the first S40 after starting, the MPU 2 starts the transmission of the band print data from the communication interface 1 to the image buffer 3. Then, the MPU 2 transmits the received band print data to the image buffer 3 by an interrupt whenever the communication interface 1 receives a new band print data. At that time, the MPU 2 independently stores each band print data in any space area in the image buffer 3 (including storage areas of print data already read into the VIF 4).

In the next S41, the MPU 2 instructs the first VIF 4-1 to read the first band print data stored in the image buffer 3.

In the next S42, the MPU 2 instructs the selection integration circuit 6 to execute the selection action.

Concretely, it is instructed to select the image signal transmitted from the first VIF4-1.

Next, the MPU 2 executes a loop process of S43 through S47 in order to execute the printing corresponding to each band print data. In the first S43 after entering the loop process, the MPU 2 instructs the selection integration circuit 6, the VIF 4 selected by the selection integration circuit 6 (the first VIF 4-1 when a number of executed times of the loop process is odd, and the second VIF 4-2 when a number of executed times of the loop process is even), the image processing circuit 5 selected by the selection integration circuit 6 (the first image processing circuit 5-1 when a number of executed times of the loop process is odd, and the second image processing circuit 5-2 when a number of executed times of the loop process is even), and the print mechanism 7 to start a printing. When the number of executed times of the loop process is odd, the first VIF 4-1 receiving the instruction of printing start, as shown in FIG. 11, reads odd-numbered band print data and transmits image data for several lines to the selection integration circuit 6 through the image processing circuit 5-1. On the contrary, when the number of executed times of the loop process is even, as shown in FIG. 12, the second VIF 4-2 which receives the instruction of the printing start, reads even-numbered band printing data and transmits image signals for

several lines to the selection integration circuit 6 through the second image processing circuit 5-2. On the other hand, the selection integration circuit 6, when the number of executed times of the loop process is odd, selects the image signals received through the first image processing circuit 5-1 and transmits them to the print mechanism 7, and when the number of executed times of the loop process is even, selects the image signals received through the second image processing circuit 5-2 and transmits them to the print mechanism 7. The print mechanism 7 prints an image corresponding to the image signal received from the selection integration circuit 6 on a sheet of paper. After this printing, the print mechanism 7 transmits the synchronous signal to the first VIF 4-1 when the number of executed times of the loop process is odd, and the synchronous signal is transmitted to the second VIF 4-2 when the number of executed times of the loop process is even. The first VIF 4-1 or the second VIF 4-2, which receives the synchronous signal, transmits an image signal of the next line to the selection integration circuit 6 so long as there is an image signal not yet transmitted.

In the next S44, the MPU 2 instructs the other VIF 4 (the second VIF 4-2 when the number of executed times of the loop process is odd, and the first VIF 4-1 when the number of executed times of the loop process is even) to read the next band print data stored in the

image buffer.

In the next S45, the MPU 2 waits until the VIF 4 transmitting image signals terminates transmission of all image signals corresponding to each band print data. Then, the MPU 2 advances the process to S46 when the transmission of all image signals corresponding to each band print data terminates.

In the S46, the MPU 2 checks whether or not all band printing data stored in the buffer 3 are completely read. The MPU 2 returns the process to the S43 after instructing the selection integration circuit 6 to select the image signal transmitted from the other VIF 4 in the S47 when all band print data are not completely read.

On the contrary, the MPU 2 terminates this control process when all band print data stored in the buffer 3 are completely read.

In this way, according to the operational example 5, two VIFs 4 are alternatively assigned every band in order to execute the band printing. Accordingly, while one VIF 4 acts, the other VIF 4 stops, therefore, it is possible to set the stopped VIF by taking a sufficient time without giving an effect to the acting VIF4. Then, the other VIF 4 promptly inherits the process when the acting VIF 4 stops after finishing the transmission of image signals. As a result, there is no case in that the printed image breaks off.

As explained in each operational example, the printer of this embodiment is provided with a plurality of VIFs 4 and image processing circuits 5, therefore, it is possible to independently store a plurality of print data for printing an image for one page in the image buffer 3 and to integrate them into a piece of print data for one page by the selection integration circuit 6, thereby printing the image on one page.

As above described, according to the printer of the present invention, it is possible to independently process a plurality of print data, each of the print data corresponding to each part to be an image printed on one page, and to print the image on one page based on these print data.

This invention being thus described, it will be obvious that same may be varied in various ways. Such variations are not to be regarded as departure from the spirit and scope of the invention, and all such modifications would be obvious for one skilled in the art intended to be included within the scope of the following claims.

What is claimed is:

1. A printer outputting a plurality of print data corresponding to am image to be printed on a same page, each of the print data having an attribute, said printer comprising:

an image buffer storing each of the print data in accordance with the attribute;

a plurality of video interfaces, each of said video interfaces reading each of said print data stored in the image buffer;

a print data integration circuit integrating the plurality of print data read by the video interfaces into a piece of print data for the same page; and

an output mechanism outputting the image of the same page based on the print data integrated by the print data integration circuit.

2. A printer according to Claim 1, wherein the plurality of print data stored in the image buffer contain form print data corresponding to a form and text print data corresponding to a text to be printed over the form.

3. A printer according to Claim 1, further comprising:

separation means for separating print data

corresponding to an image with an text into print data corresponding to the image and print data corresponding to the text; and

storage means for storing each of the print data separated by said separation means in the image buffer in accordance with the attribute.

4. A printer according to Claim 3, further comprising:

a plurality of image processing circuits, each of said image processing circuits applying each image process to each of the print data read by each of said video interfaces.

5. A printer according to Claim 1, wherein the plurality of print data stored in the image buffer are obtained by dividing print data corresponding to the image to be printed on the same page into a plurality of bands, and wherein said print data integration circuit repeatedly selects each of said print data read by each of said video interfaces and outputs selected print data to the output mechanism.

6. A controller controlling a plurality of print data, each of the print data having an attribute, said controller comprising:

a plurality of video interfaces, each of said video

interfaces reading each of said print data stored in an image buffer storing each of the print data in accordance with the attribute; and

a print data integration circuit integrating the plurality of print data read by the video interfaces into a piece of print data for the same page.

7. A controller according to Claim 6, wherein the plurality of print data stored in the image buffer contain form print data corresponding to a form and text print data corresponding to a text to be printed over the form.

8. A controller according to Claim 6, further comprising:

separation means for separating print data corresponding to an image with an text into print data corresponding to the image and print data corresponding to the text; and

storage means for storing each of the print data separated by said separation means in the image buffer in accordance with the attribute.

9. A controller according to Claim 8, further comprising:

a plurality of image processing circuits, each of said image processing circuits applying each image

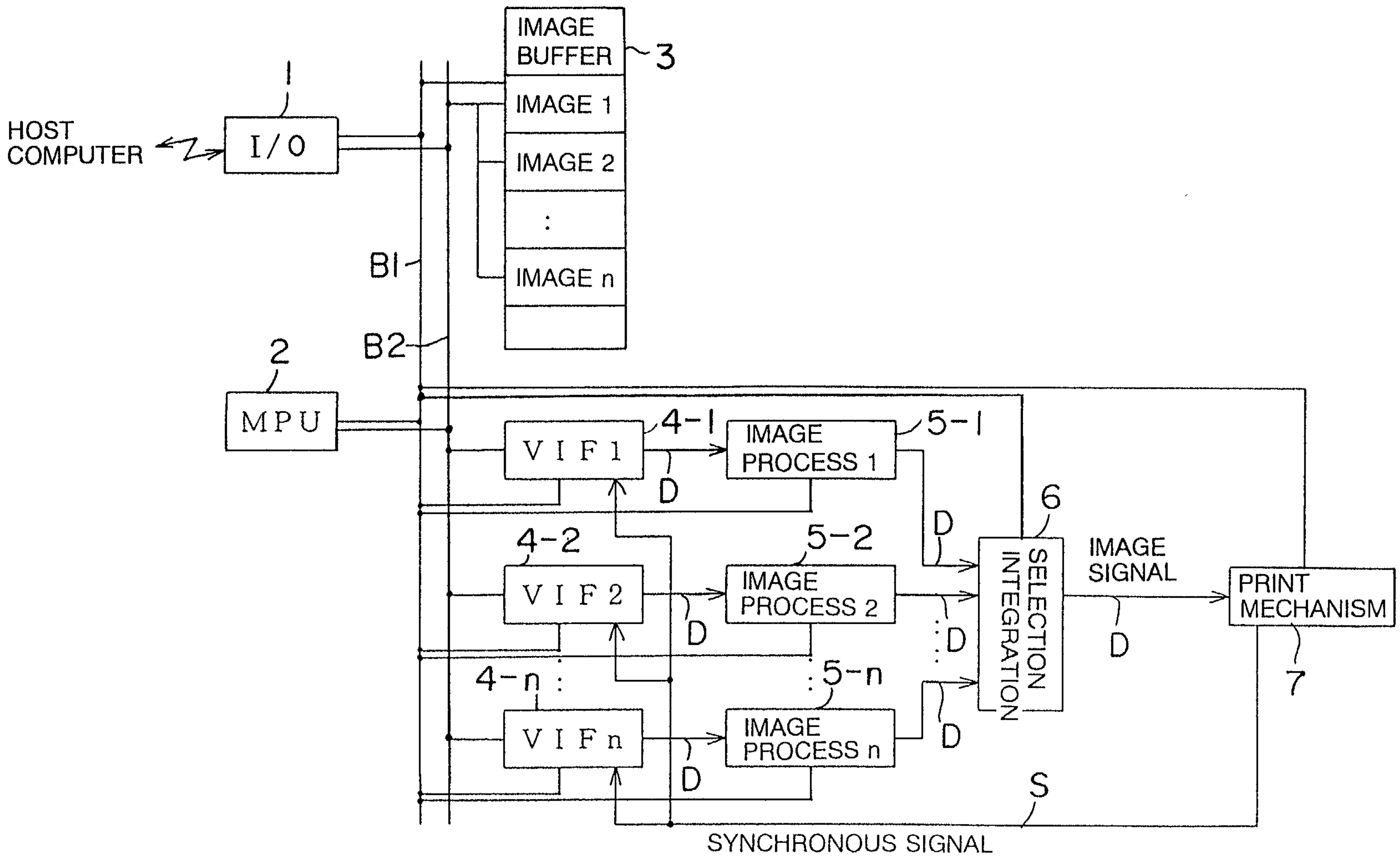
process to each of the print data read by each of said video interfaces.

10. A controller according to Claim 6, wherein the plurality of print data stored in the image buffer are obtained by dividing print data corresponding to the image to be printed on the same page into a plurality of bands, and wherein said print data integration circuit repeatedly selects each of said print data read by each of said video interfaces and outputs selected print data to the output mechanism.

ABSTRACT OF THE DISCLOSURE

The present invention provides a printer capable of separately processing a plurality of print data corresponding to am image to be printed on a same page, each of the print data having an attribute, in accordance with the attribute. The printer comprises an image, a plurality of video interfaces, a print data integration circuit, and an output mechanism. The image buffer stores each of the print data in accordance with the attribute. Each of the video interfaces reads each of the print data stored in the image buffer. The print data integration circuit integrates the plurality of print data read by the video interfaces into a piece of print data for the same page. The output mechanism outputs the image of the same page based on the print data integrated by the print data integration circuit. Therefore, the plurality of print data can be separately processed and outputted in accordance with the attribute.

FIG. 1



HOST
COMPUTER
1
I/O
2
MPU
B1
B2
IMAGE
BUFFER
3
IMAGE 1
IMAGE 2
:
IMAGE n
VIF1
4-1
VIF2
4-2
4-n
VIFn
D
IMAGE
PROCESS 1
5-1
IMAGE
PROCESS 2
5-2
5-n
IMAGE
PROCESS n
SELECTION
INTEGRATION
6
IMAGE
SIGNAL
PRINT
MECHANISM
7
S
SYNCHRONOUS SIGNAL

FIG. 2

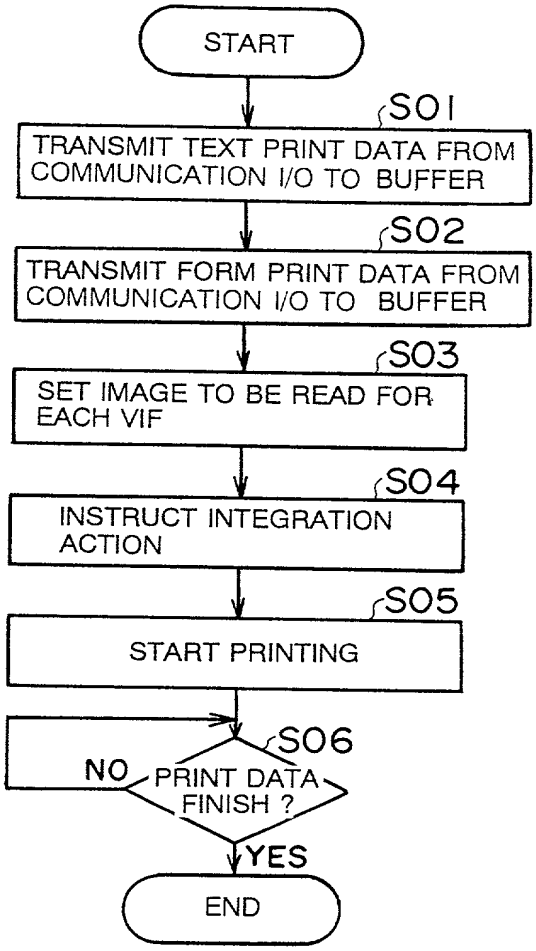

START
S01
TRANSMIT TEXT PRINT DATA FROM COMMUNICATION I/O TO BUFFER
S02
TRANSMIT FORM PRINT DATA FROM COMMUNICATION I/O TO BUFFER
S03
SET IMAGE TO BE READ FOR EACH VIF
S04
INSTRUCT INTEGRATION ACTION
S05
START PRINTING
S06
NO
PRINT DATA FINISH ?
YES
END

FIG. 3

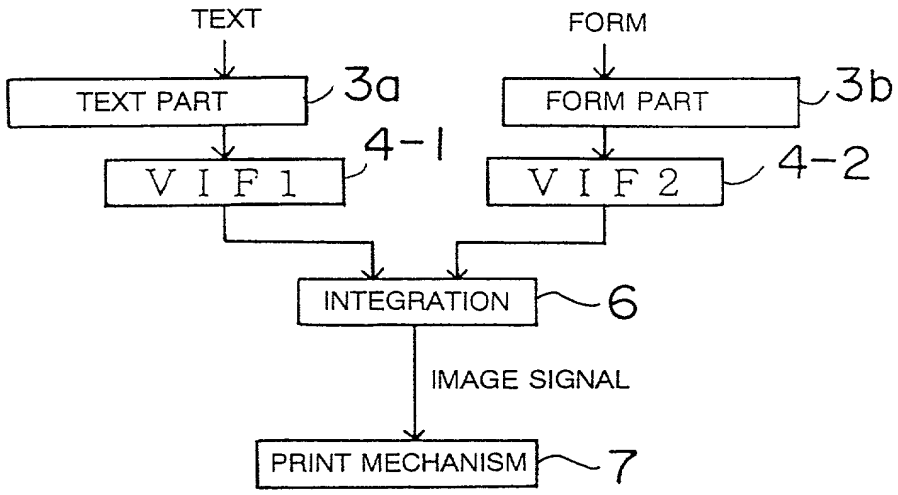

TEXT
FORM
TEXT PART
3a
FORM PART
3b
V I F 1
4-1
V I F 2
4-2
INTEGRATION
6
IMAGE SIGNAL
PRINT MECHANISM
7

FIG. 4

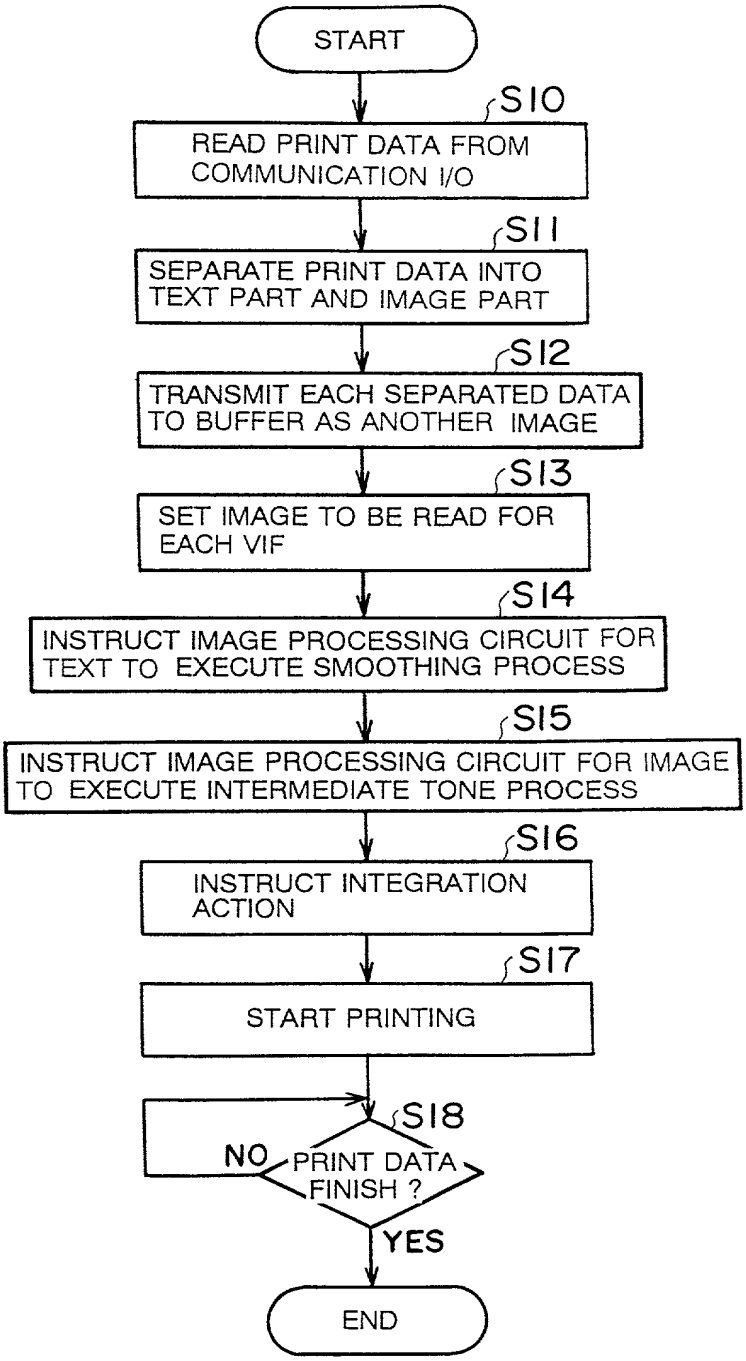

START
S10
READ PRINT DATA FROM COMMUNICATION I/O
S11
SEPARATE PRINT DATA INTO TEXT PART AND IMAGE PART
S12
TRANSMIT EACH SEPARATED DATA TO BUFFER AS ANOTHER IMAGE
S13
SET IMAGE TO BE READ FOR EACH VIF
S14
INSTRUCT IMAGE PROCESSING CIRCUIT FOR TEXT TO EXECUTE SMOOTHING PROCESS
S15
INSTRUCT IMAGE PROCESSING CIRCUIT FOR IMAGE TO EXECUTE INTERMEDIATE TONE PROCESS
S16
INSTRUCT INTEGRATION ACTION
S17
START PRINTING
S18
NO
PRINT DATA FINISH ?
YES
END

FIG. 5

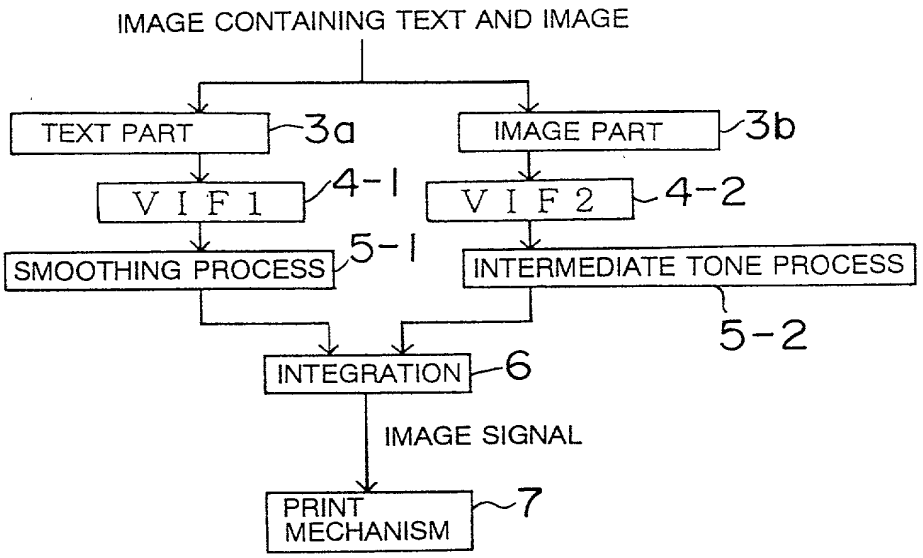


IMAGE CONTAINING TEXT AND IMAGE
TEXT PART
3a
IMAGE PART
3b
V I F 1
4-1
V I F 2
4-2
SMOOTHING PROCESS
5-1
INTERMEDIATE TONE PROCESS
5-2
INTEGRATION
6
IMAGE SIGNAL
PRINT MECHANISM
7

FIG. 6

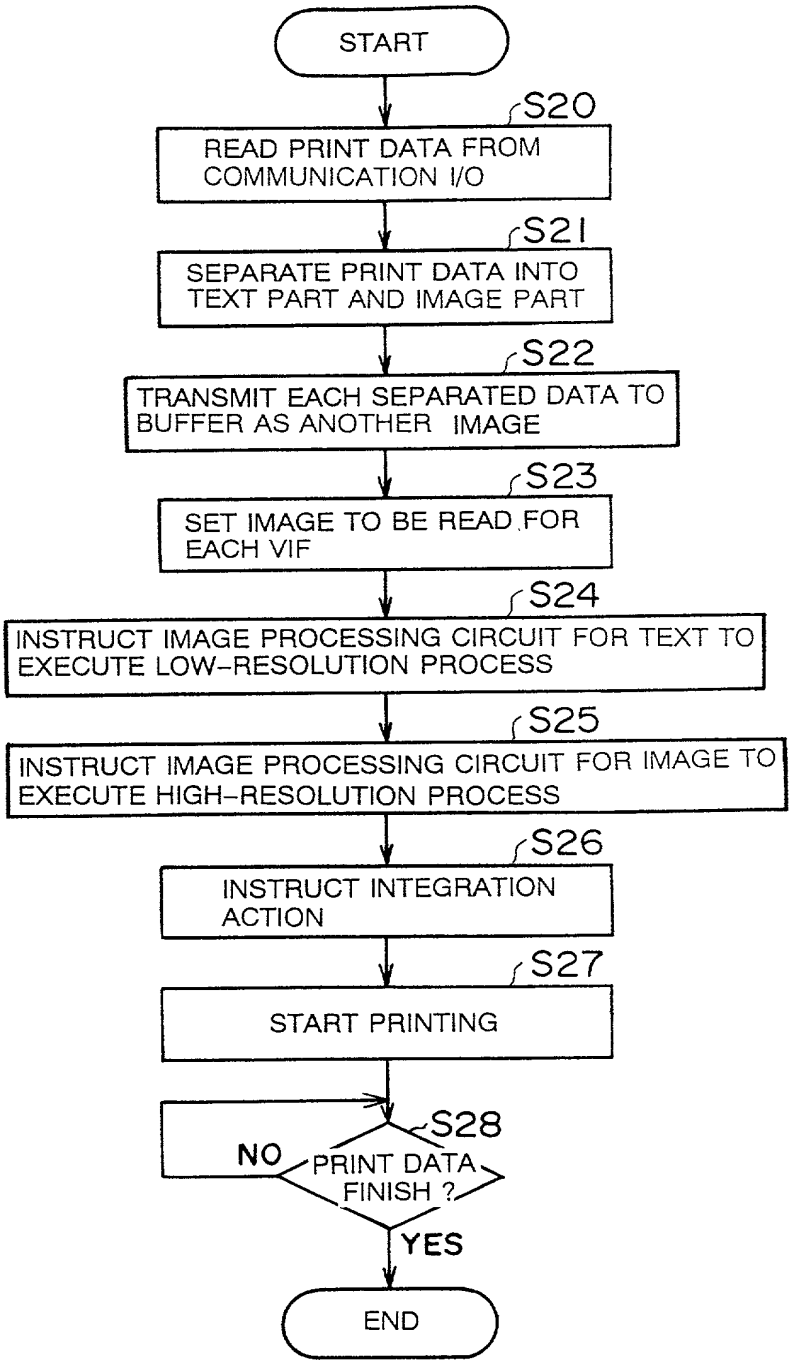

START
S20
READ PRINT DATA FROM COMMUNICATION I/O
S21
SEPARATE PRINT DATA INTO TEXT PART AND IMAGE PART
S22
TRANSMIT EACH SEPARATED DATA TO BUFFER AS ANOTHER IMAGE
S23
SET IMAGE TO BE READ FOR EACH VIF
S24
INSTRUCT IMAGE PROCESSING CIRCUIT FOR TEXT TO EXECUTE LOW-RESOLUTION PROCESS
S25
INSTRUCT IMAGE PROCESSING CIRCUIT FOR IMAGE TO EXECUTE HIGH-RESOLUTION PROCESS
S26
INSTRUCT INTEGRATION ACTION
S27
START PRINTING
S28
NO
PRINT DATA FINISH ?
YES
END

FIG. 7

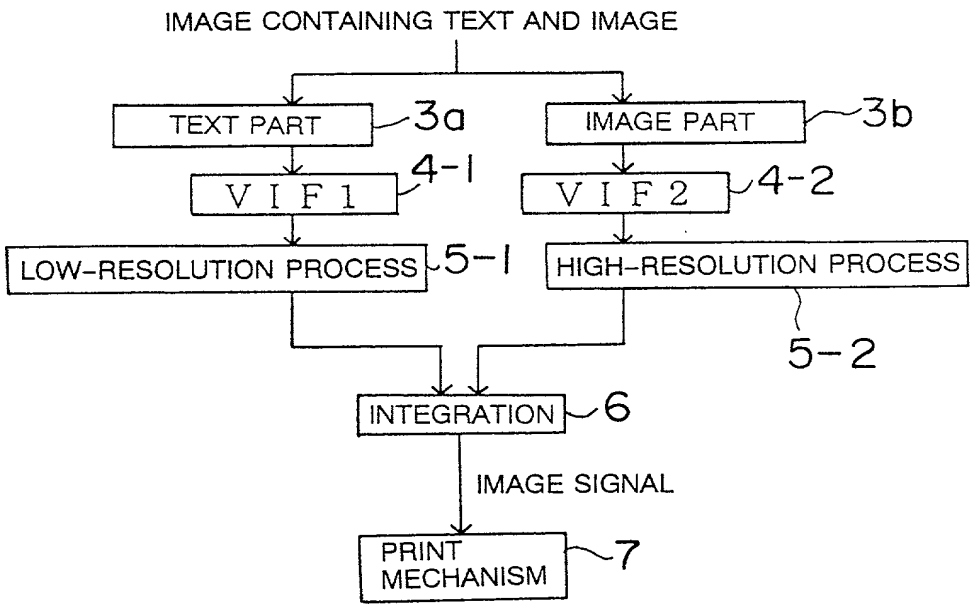


IMAGE CONTAINING TEXT AND IMAGE
TEXT PART
3a
IMAGE PART
3b
V I F 1
4-1
V I F 2
4-2
LOW-RESOLUTION PROCESS
5-1
HIGH-RESOLUTION PROCESS
5-2
INTEGRATION
6
IMAGE SIGNAL
PRINT MECHANISM
7

FIG. 8

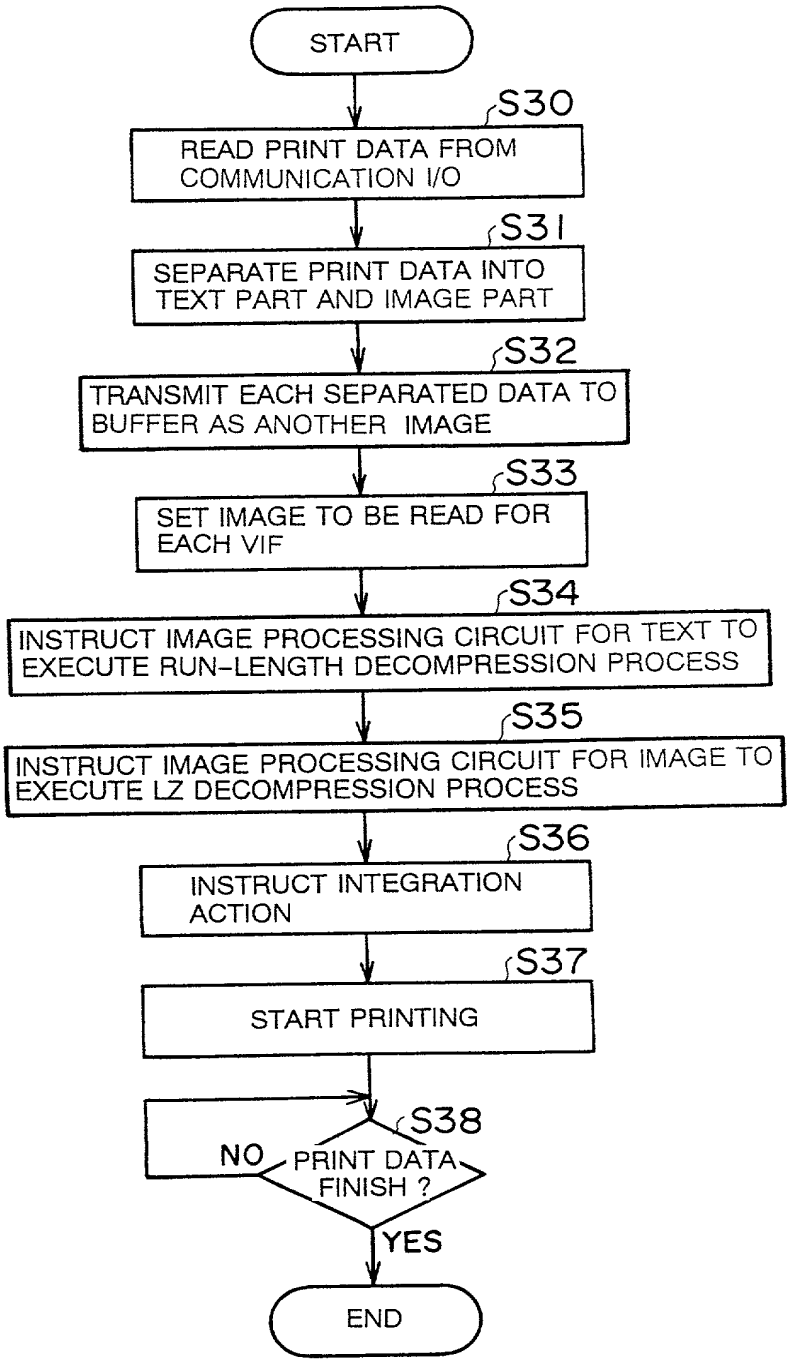

START
S30
READ PRINT DATA FROM COMMUNICATION I/O
S31
SEPARATE PRINT DATA INTO TEXT PART AND IMAGE PART
S32
TRANSMIT EACH SEPARATED DATA TO BUFFER AS ANOTHER IMAGE
S33
SET IMAGE TO BE READ FOR EACH VIF
S34
INSTRUCT IMAGE PROCESSING CIRCUIT FOR TEXT TO EXECUTE RUN-LENGTH DECOMPRESSION PROCESS
S35
INSTRUCT IMAGE PROCESSING CIRCUIT FOR IMAGE TO EXECUTE LZ DECOMPRESSION PROCESS
S36
INSTRUCT INTEGRATION ACTION
S37
START PRINTING
S38
NO
PRINT DATA FINISH ?
YES
END

FIG. 9

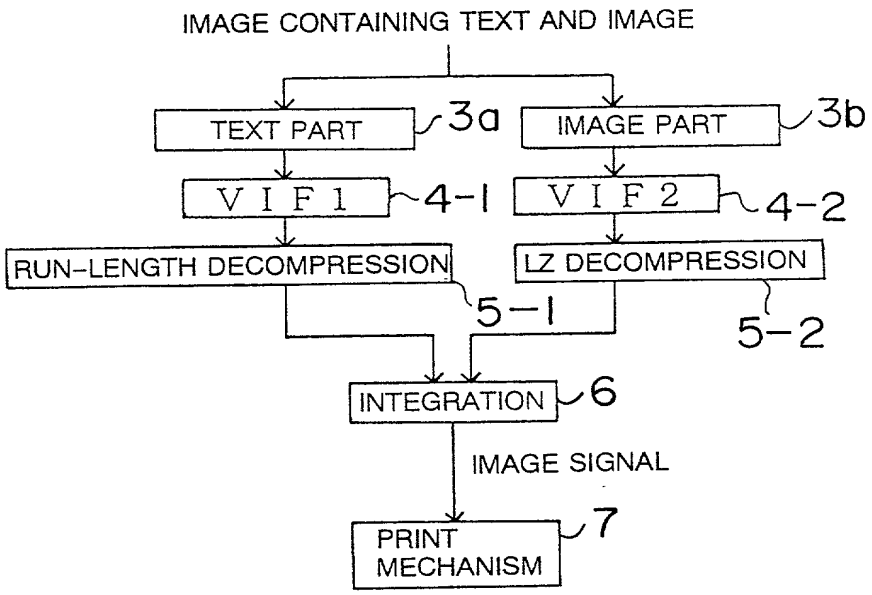


IMAGE CONTAINING TEXT AND IMAGE
TEXT PART
3a
IMAGE PART
3b
V I F 1
4-1
V I F 2
4-2
RUN-LENGTH DECOMPRESSION
LZ DECOMPRESSION
5-1
5-2
INTEGRATION
6
IMAGE SIGNAL
PRINT MECHANISM
7

FIG. 10

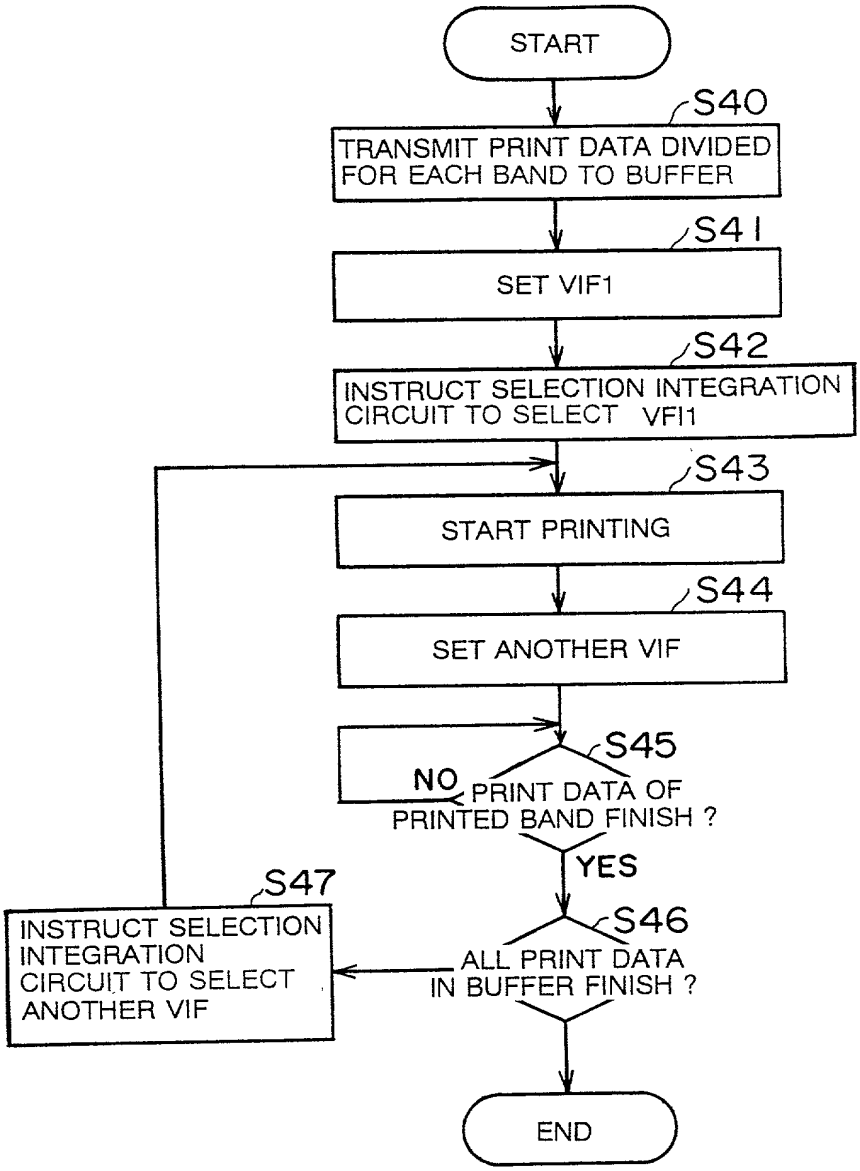

START
S40
TRANSMIT PRINT DATA DIVIDED FOR EACH BAND TO BUFFER
S41
SET VIF1
S42
INSTRUCT SELECTION INTEGRATION CIRCUIT TO SELECT VFI1
S43
START PRINTING
S44
SET ANOTHER VIF
S45
NO
PRINT DATA OF PRINTED BAND FINISH ?
YES
S46
ALL PRINT DATA IN BUFFER FINISH ?
S47
INSTRUCT SELECTION INTEGRATION CIRCUIT TO SELECT ANOTHER VIF
END

FIG. 11

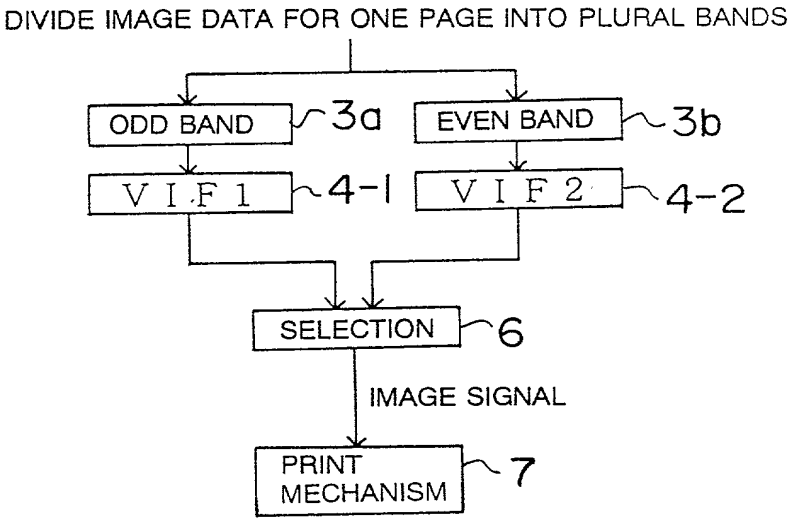
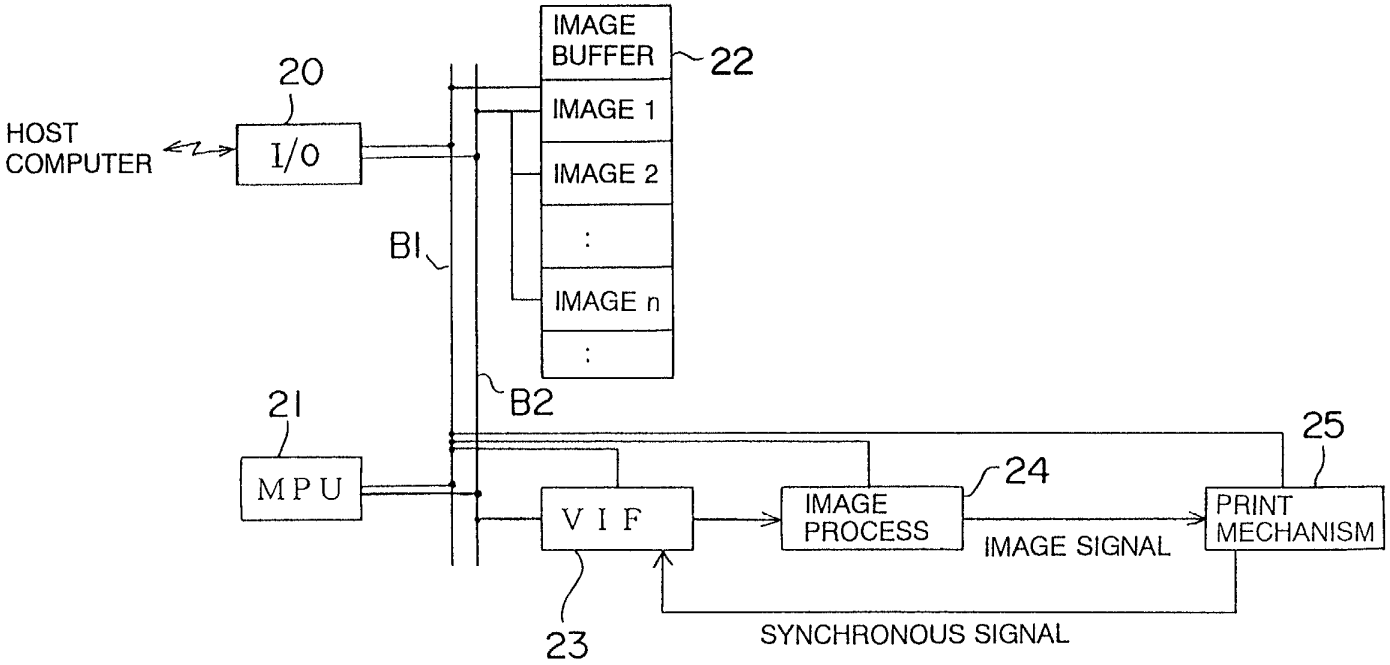

DIVIDE IMAGE DATA FOR ONE PAGE INTO PLURAL BANDS
ODD BAND
3a
EVEN BAND
3b
V I F 1
4-1
V I F 2
4-2
SELECTION
6
IMAGE SIGNAL
PRINT MECHANISM
7

FIG. 12
PRIOR ART



PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名が発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PRINTER

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、印内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
9-301897	Japan	4/November/1997	☐
			☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

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